

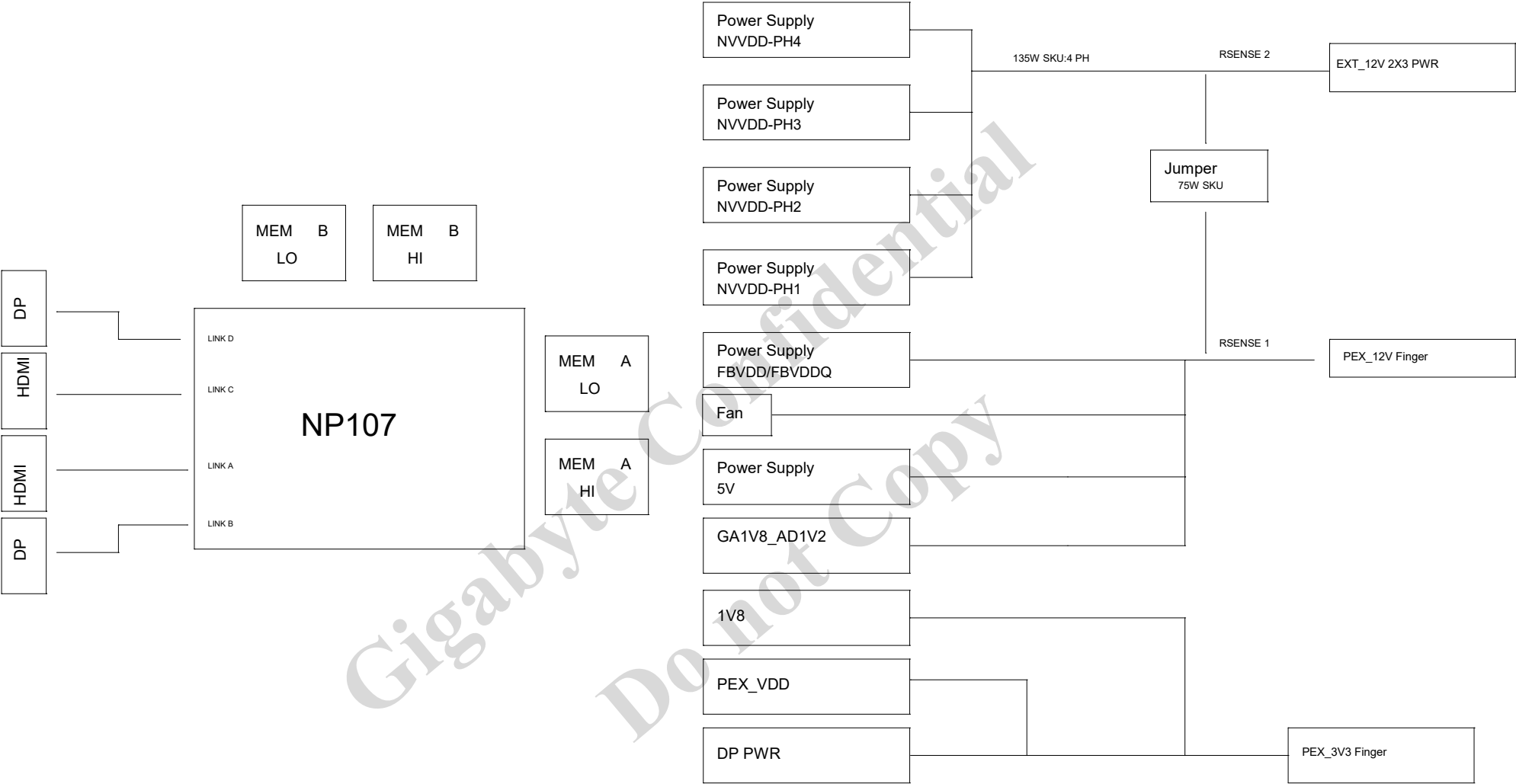
AD107 GB5C-128 4L  
128b,G6 2CHx16 IC PCB  
DP + HDMI + DP + DP

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Block Diagram



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ASSEMBLY  
PAGE DETAIL

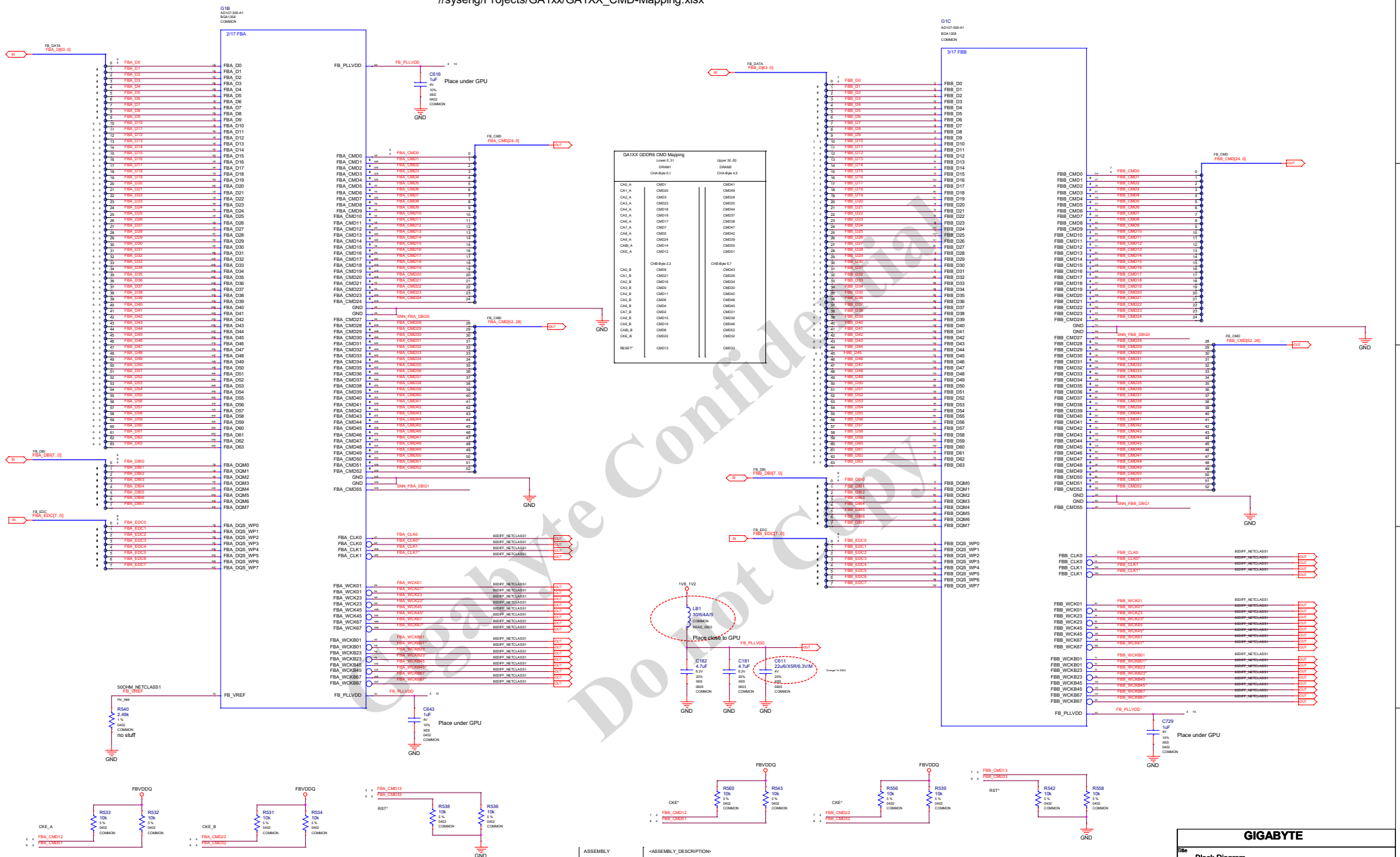
ASSEMBLY DESCRIPTION  
Block Diagram

GIGABYTE			
Title			
Block Diagram			
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		GV-N4060OC-8GL	1.0
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MEMORY: GPU Partition A/B

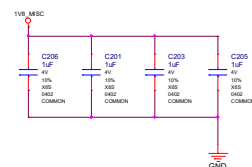
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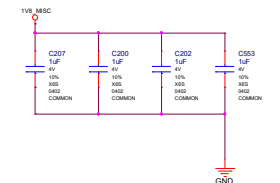
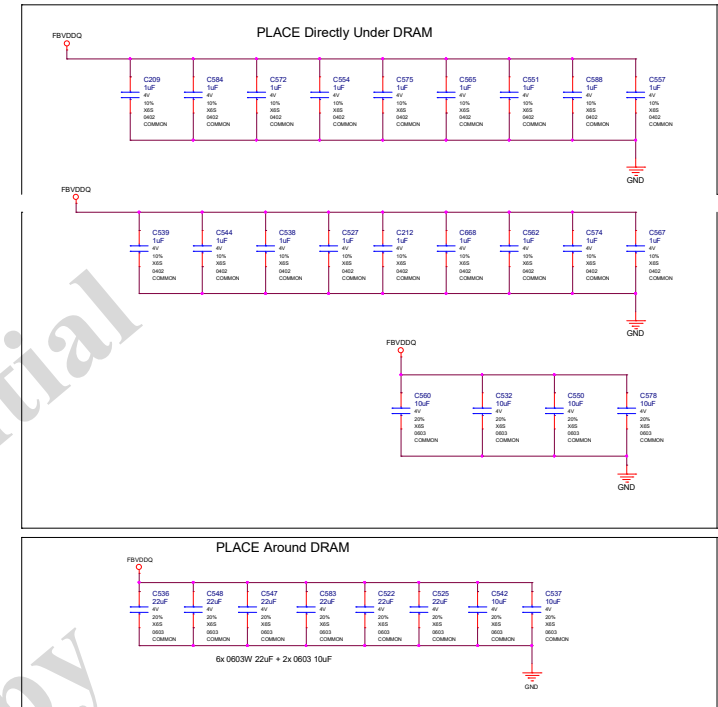
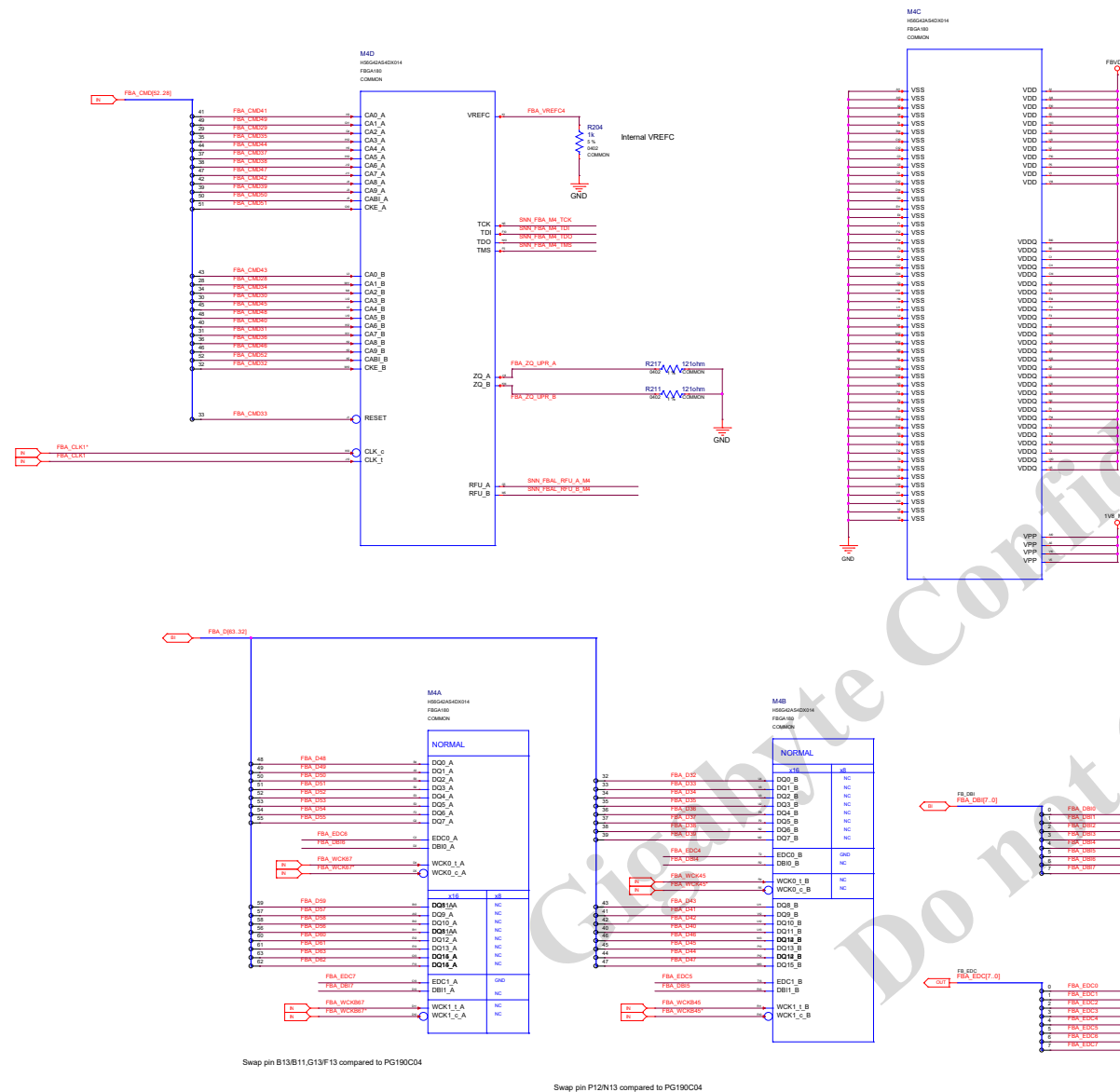


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Title			
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<ASSEMBLY\_DESCRIPTION:  
MEMORY: GPU Partition A/B





Swap pin B13/B11.G13/F13 compared to PG190C04

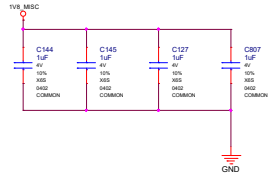
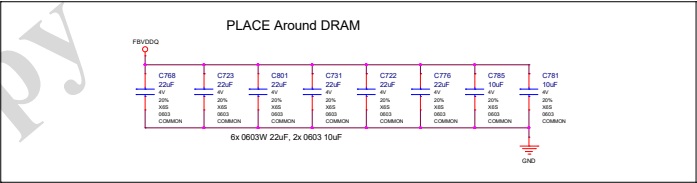
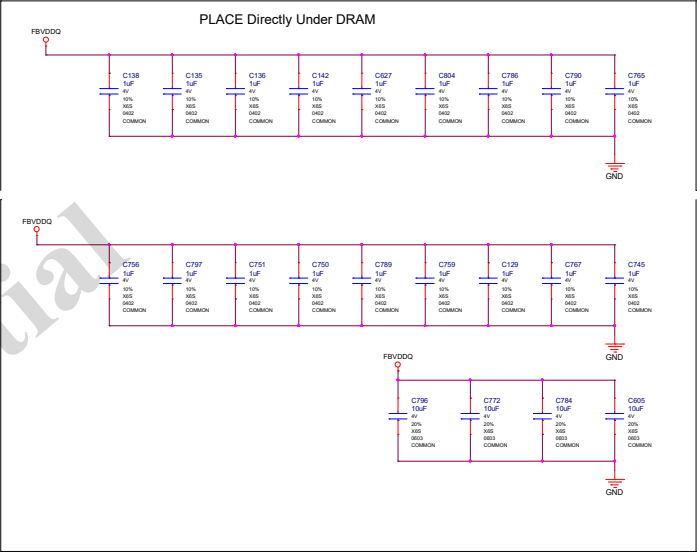
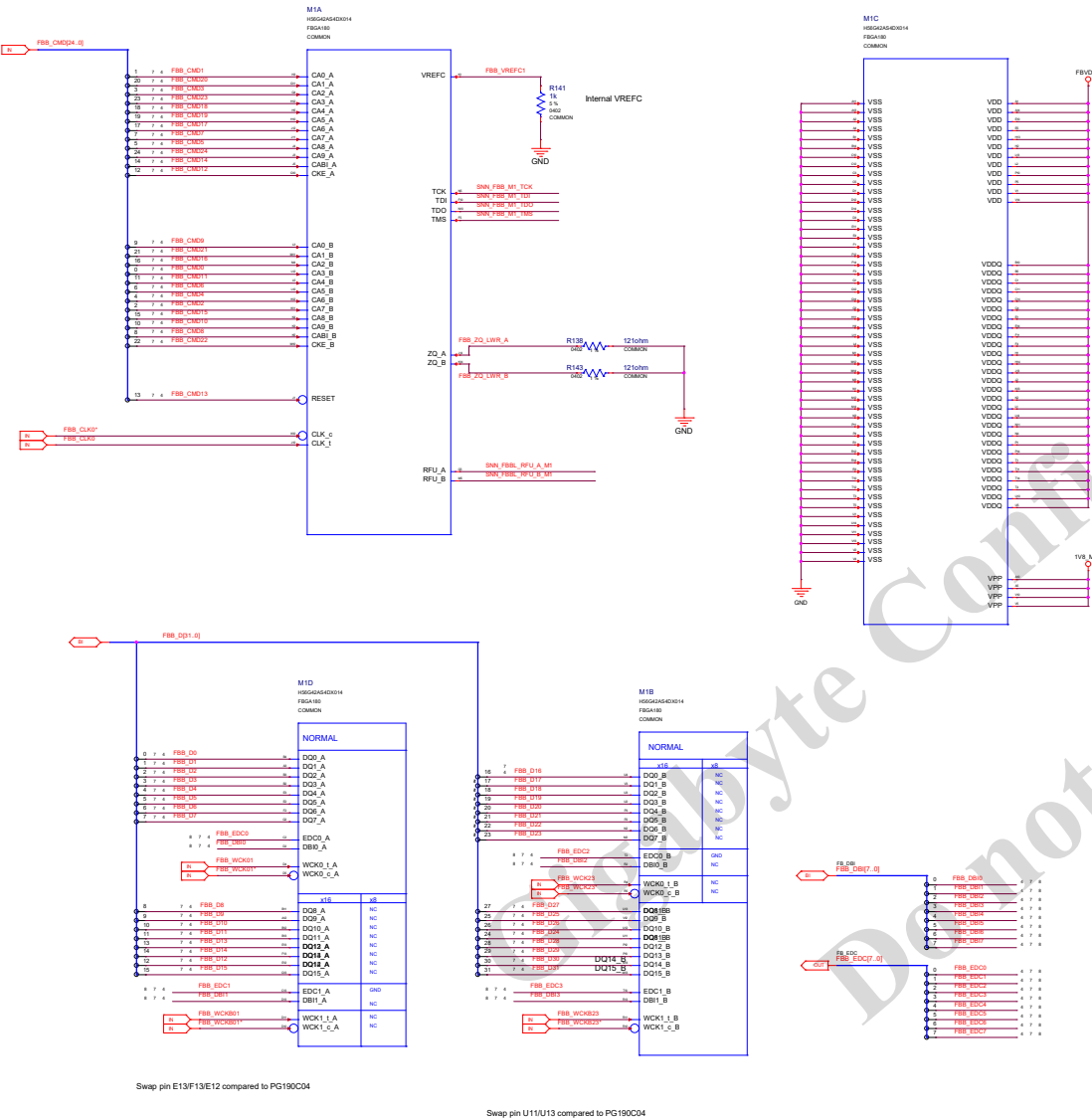
Swap pin P12/N13 compared to PG190C04

GIGABYTE			
File	Block Diagram		
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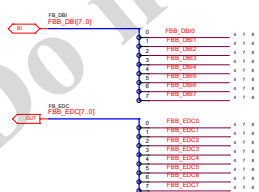
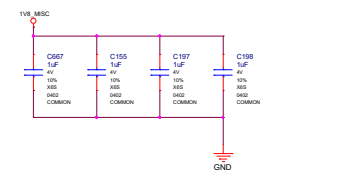
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
MEMORY: FBA Partition 63..32

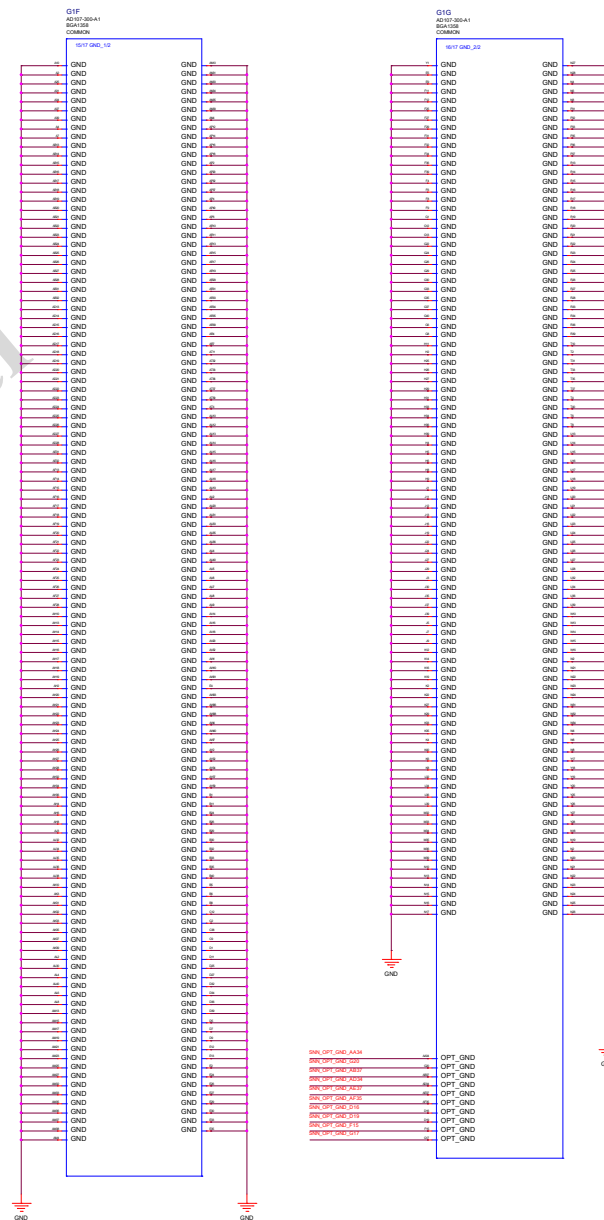
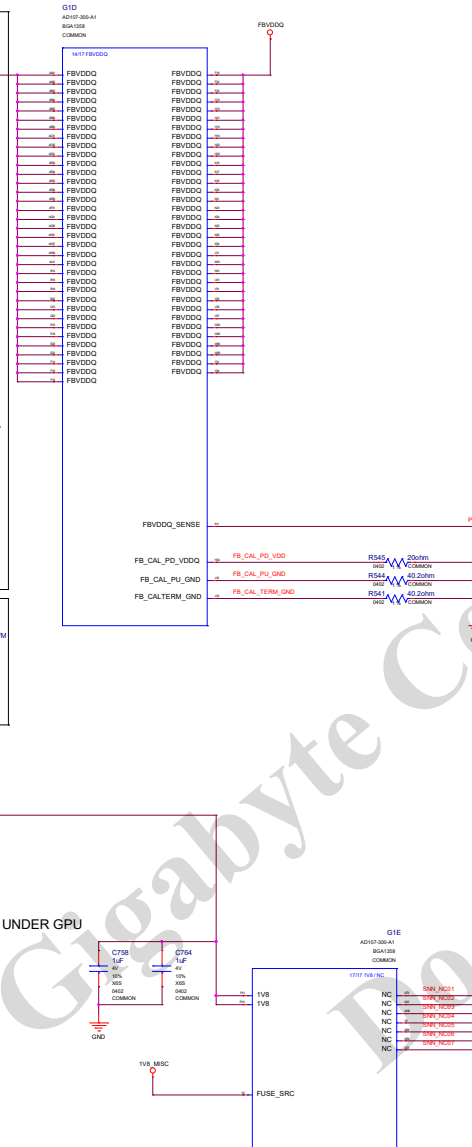
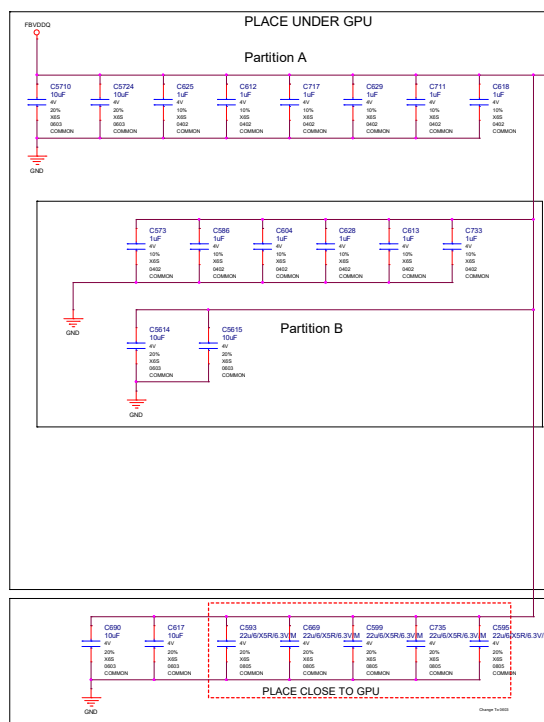


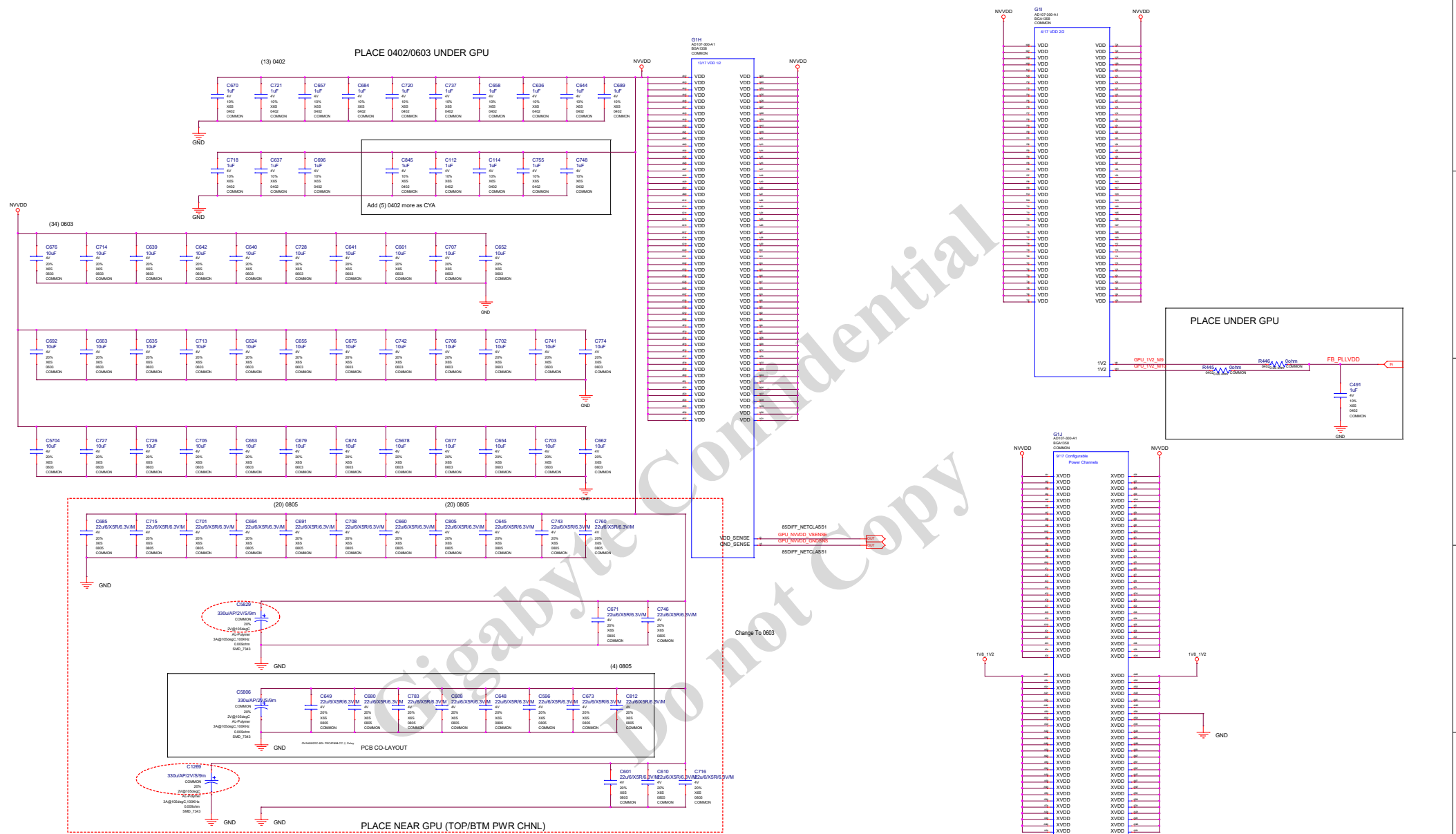
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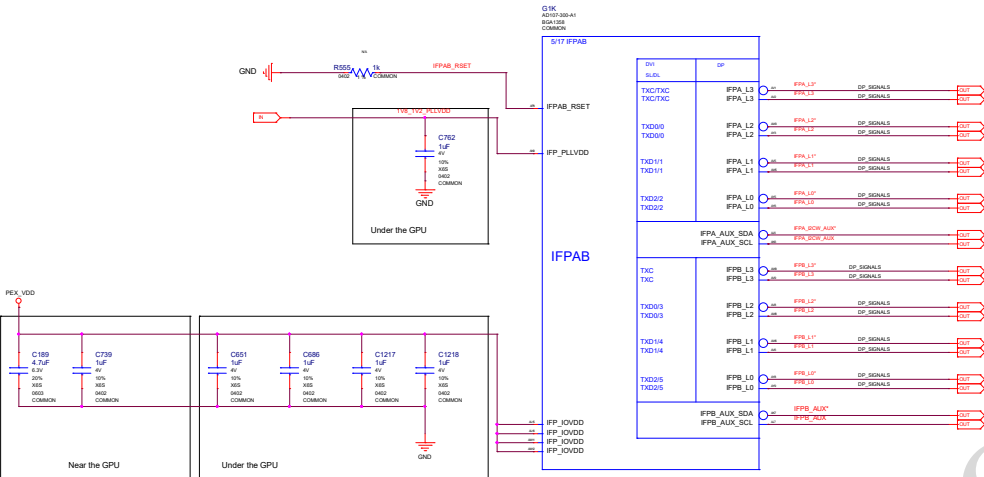


Swap pin P12/P13 compared to PG190C04









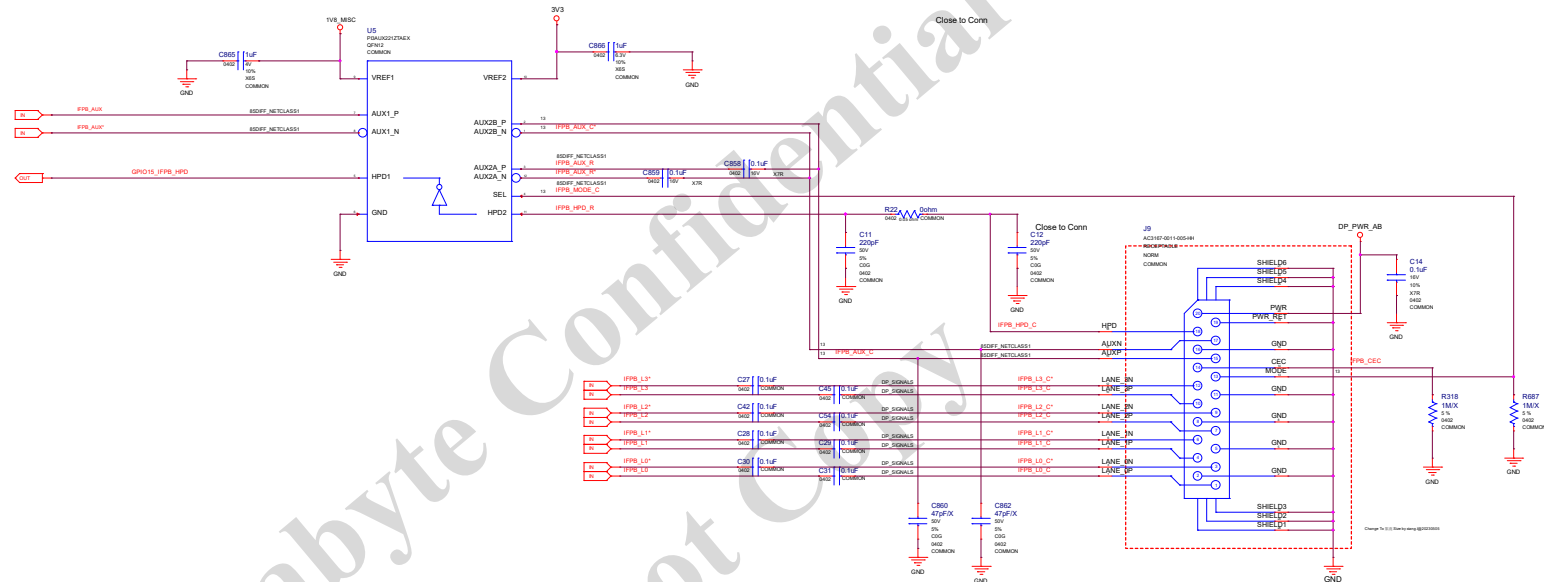
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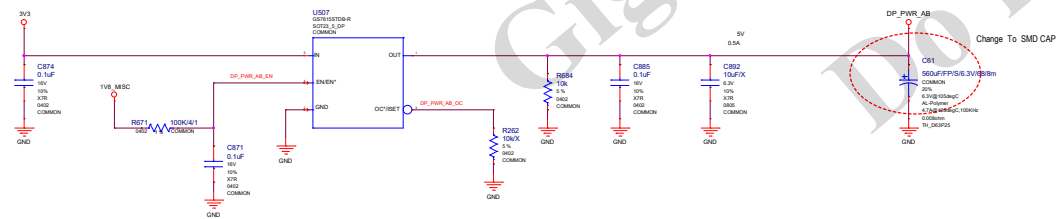


## IFPB DP

South



Fused DP PWR

ASSEMBLY  
PAGE DETAIL

<ASSEMBLY\_DESCRIPTION  
IFPB DP

## GIGABYTE

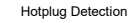
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1.

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Middle North

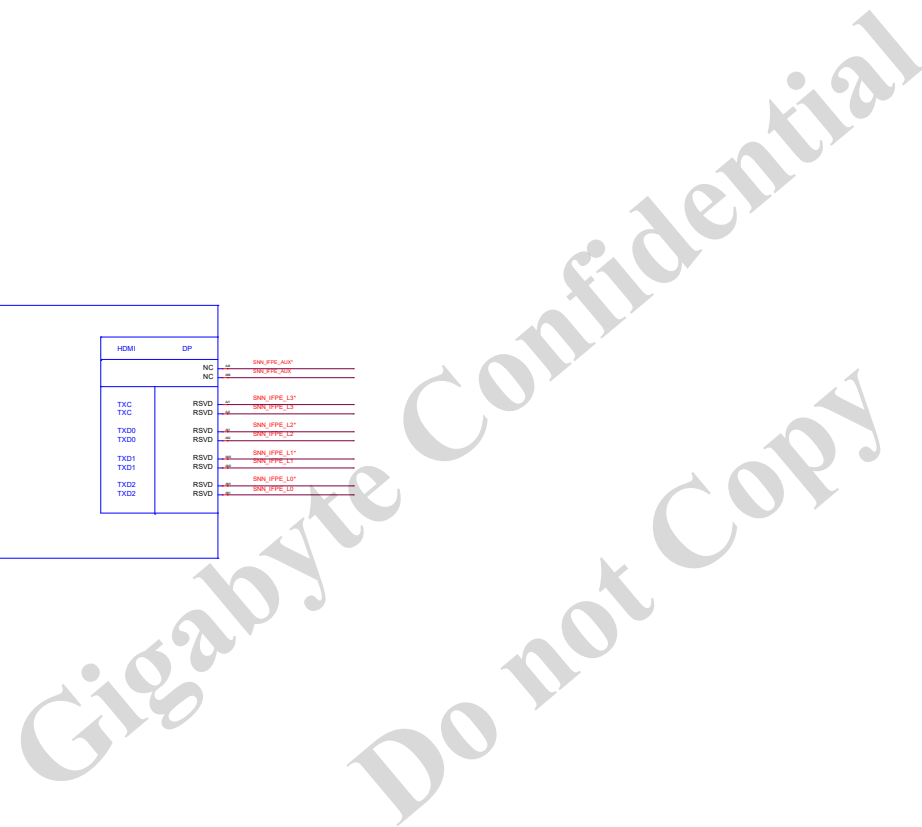


**GIGABYTE**

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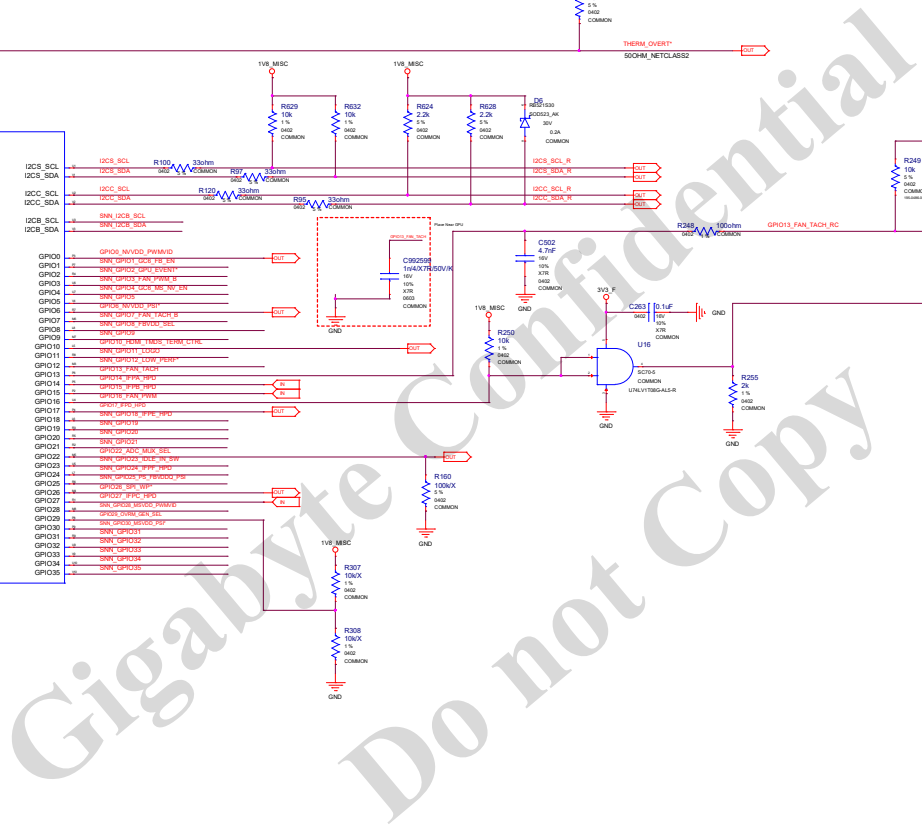
Change To SMD CAP



<b>GIGABYTE</b>			
Title <b>Block Diagram</b>			
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<b>GIGABYTE</b>			
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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	L	H	00101
L	L	M	01000
L	M	L	01001
L	M	H	01010

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	16Gb	128-bit	Samsung	C
00001	16Gb	128-bit	Micron	
00010	16Gb	128-bit	Hynix	
00011	16Gb	128-bit	Samsung	
00100	16Gb	128-bit	Micron	
00101	16Gb	128-bit	Hynix	A
01000	16Gb	128-bit	Hynix	
01001	16Gb	128-bit	Micron	C
01010	16Gb	128-bit	Samsung	

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
L	L	M	4'd8	FS_OVERT ENABLE
L	M	L	4'd9	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

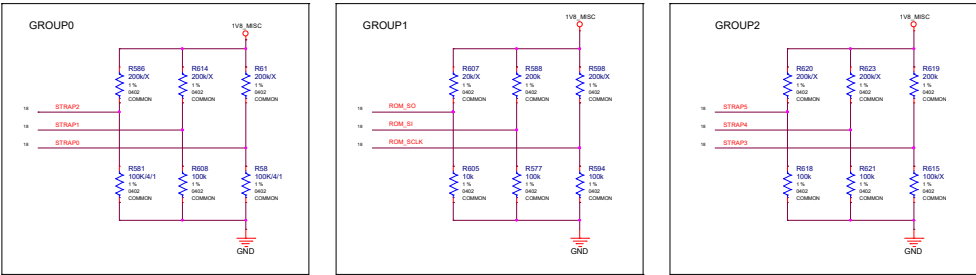
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

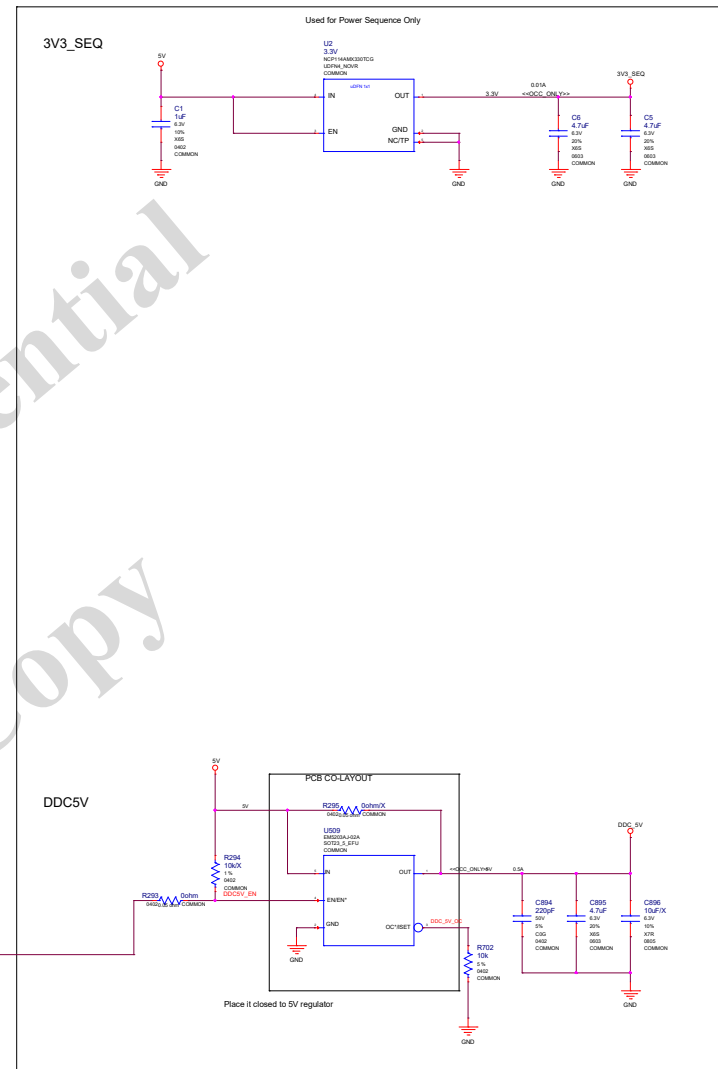
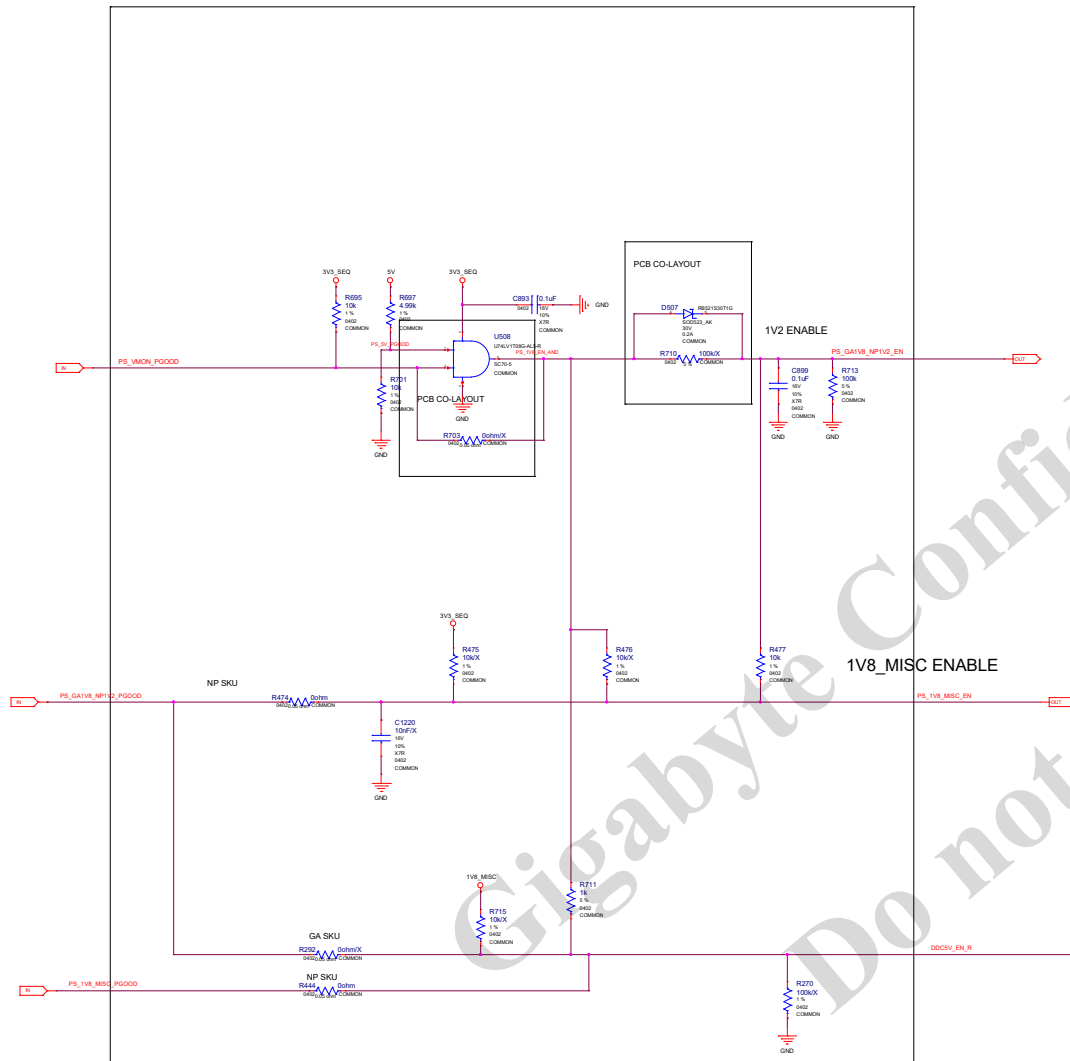
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



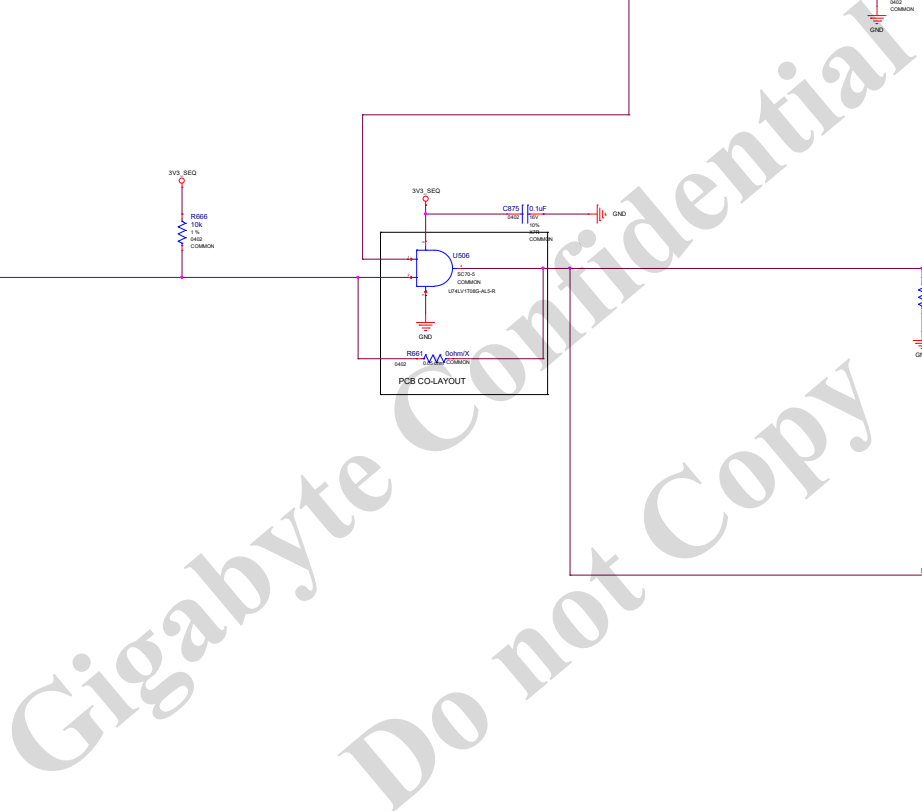
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GIGABYTE			
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ASSEMBLY PAGE DETAIL  
~ASSEMBLY DESCRIPTION~  
SEQ\_3V3\_SEQ.DDC\_5V\_DP\_AUX\_PROT



PAGE DETAIL

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Size	Document Number
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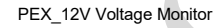
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Custom	GV-N4060OC-8G
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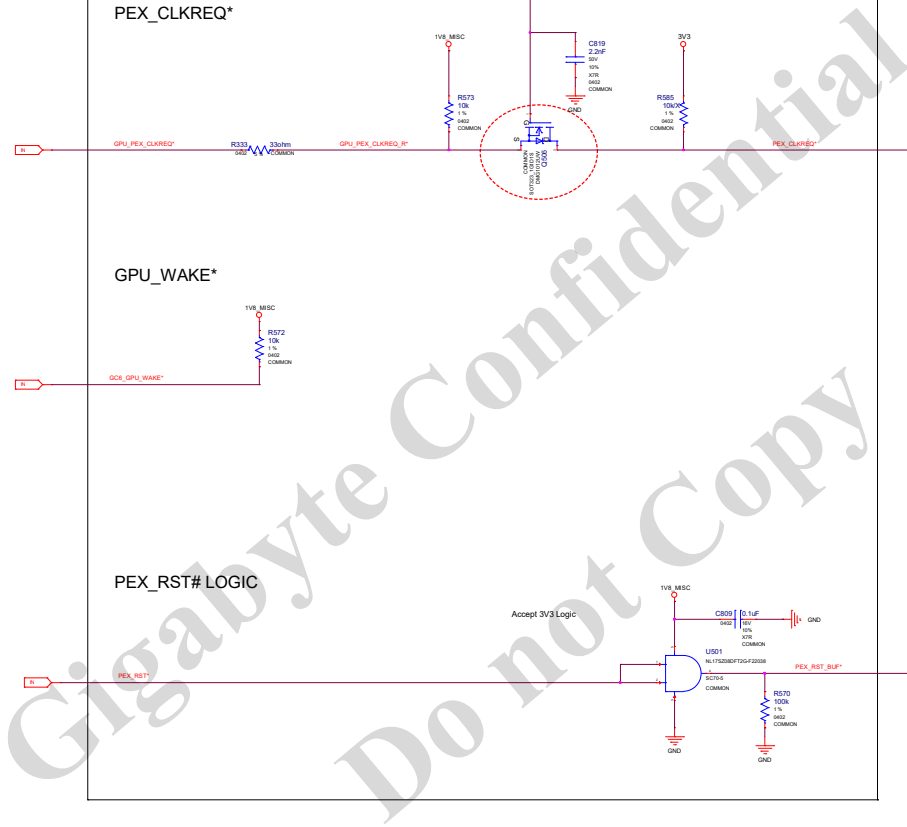
2

Route the trace to PEX Golden Finger



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: VOLTAGE MONITOR

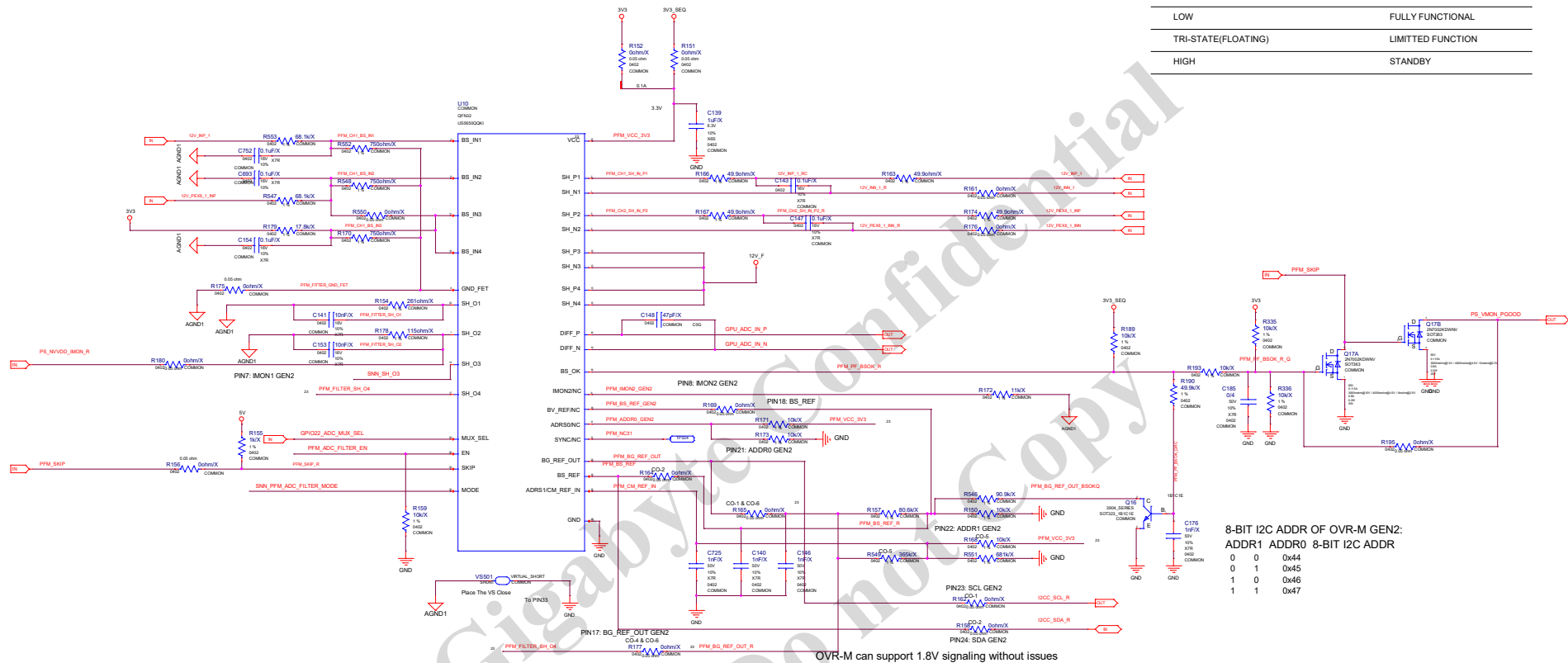
A	B	C	D	E	F	G		
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A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



OVR-M GEN2 SUPPORT

OVR-M GEN2:  
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32  
are different from GEN1 OVRM,

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ASSEMBLY PAGE DETAIL  
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PS Pre-Misc

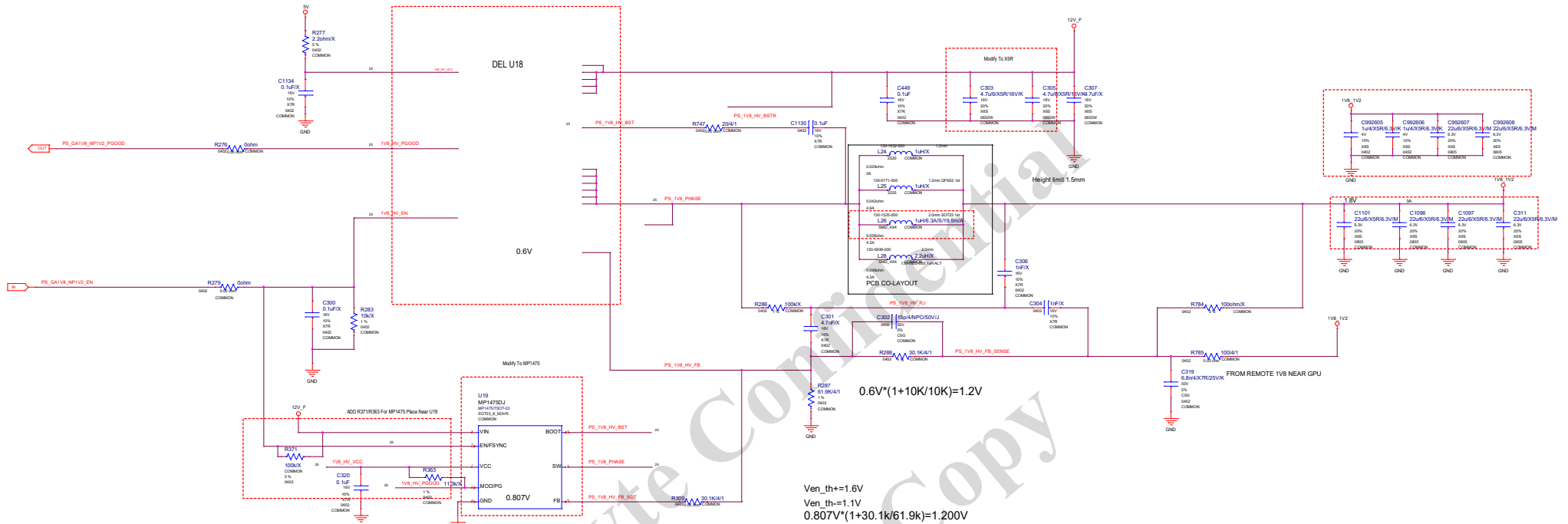
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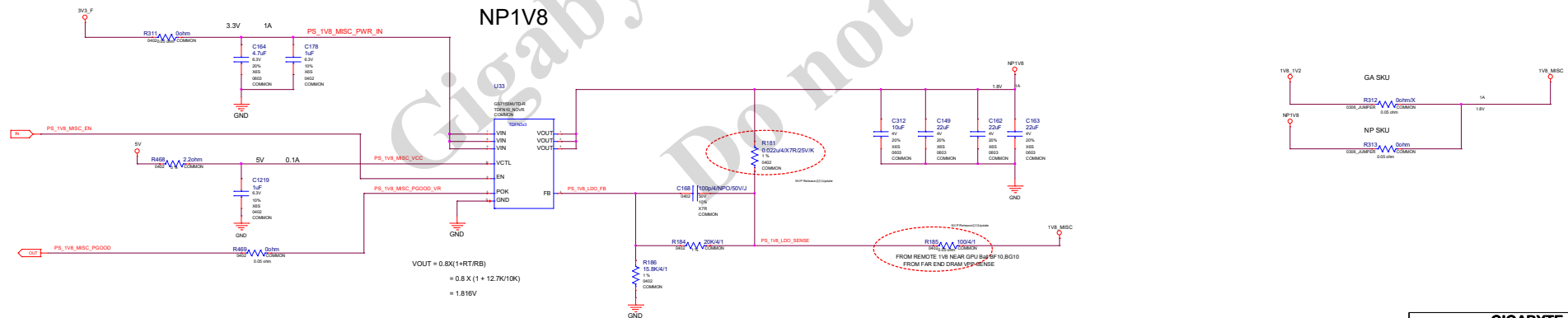
PS: 1V2

## GA1V8/NP1V2 Switcher



PS: 1V8

## NP1V8



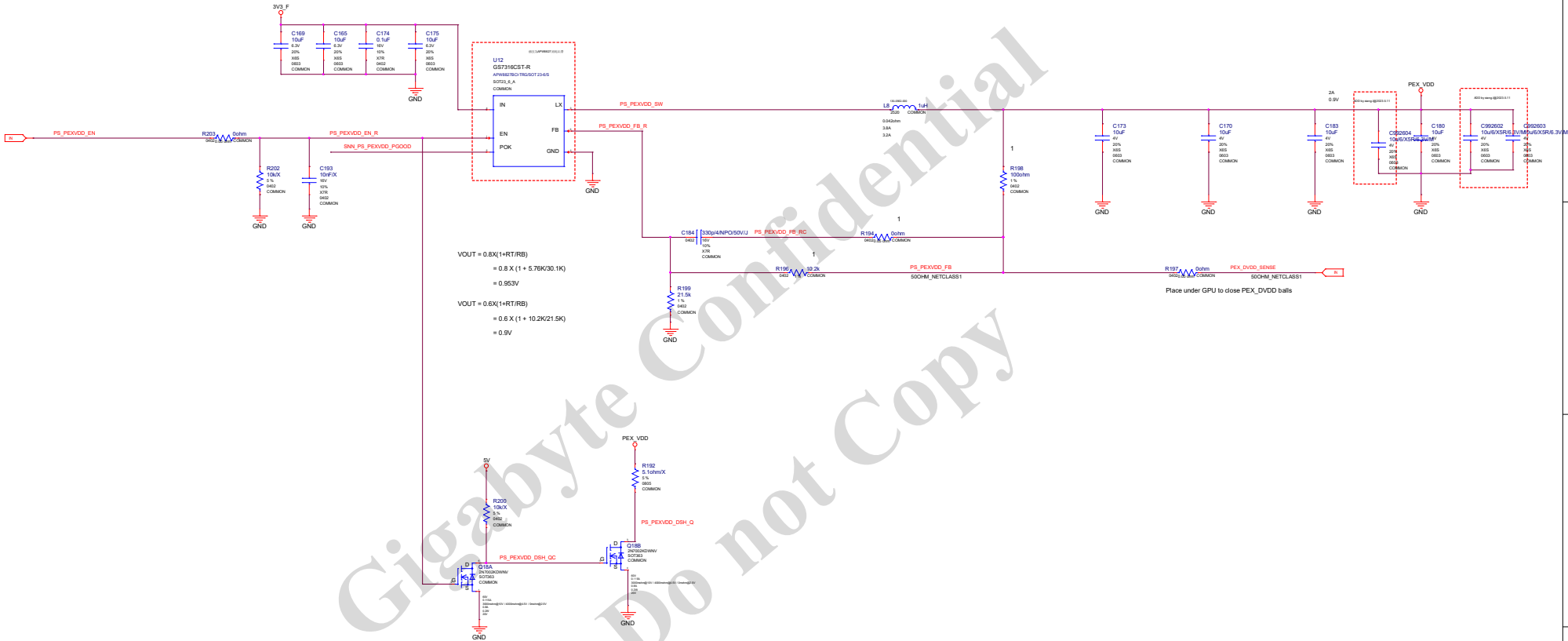
**GIGABYTE**

Title			
Block Diagram			
Size	Document Number		Rev
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION: PS: 1V8/1V2
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PS: PEXVDD

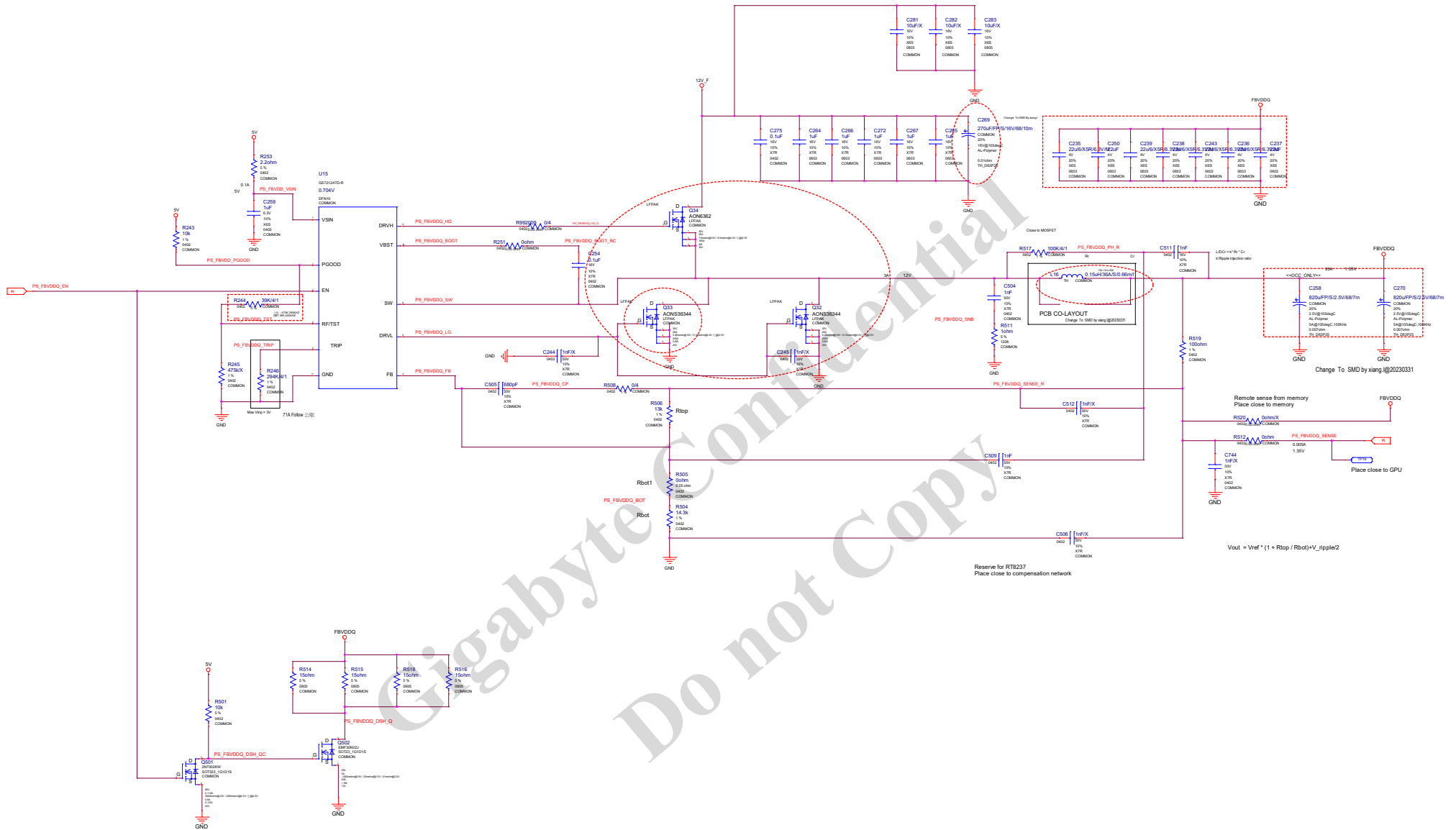


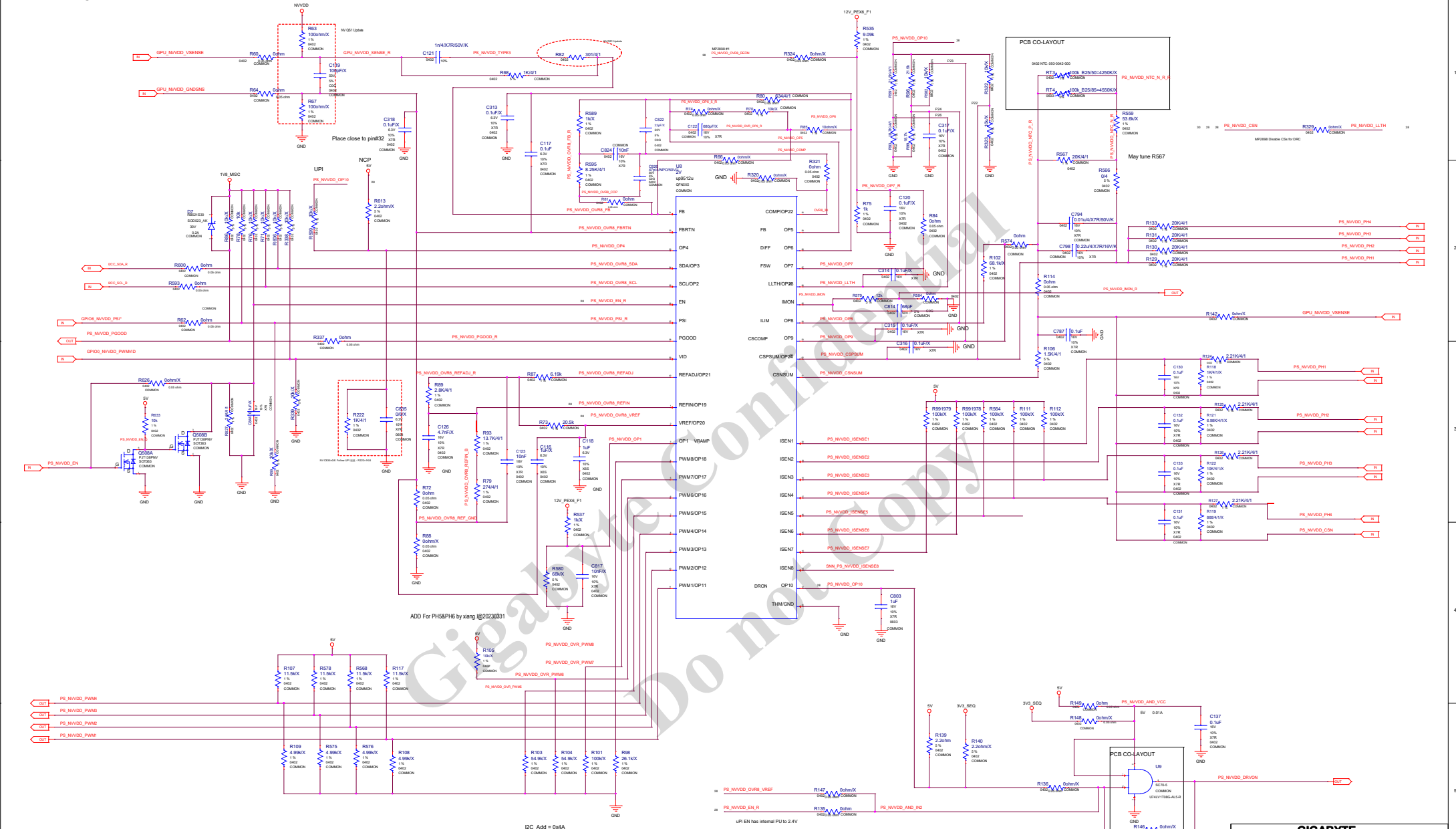
$$VOUT = 0.8X(1+RT/RB)$$
$$= 0.8X(1 + 5.76K/30.1K)$$
$$= 0.953V$$
$$VOUT = 0.6X(1+RT/RB)$$
$$= 0.6X(1 + 10.2K/21.5K)$$
$$= 0.9V$$

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ASSEMBLY PAGE DETAIL  
ASSEMBLY DESCRIPTION  
PS: PEXVDD

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Block Diagram			
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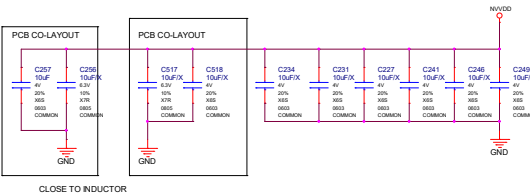
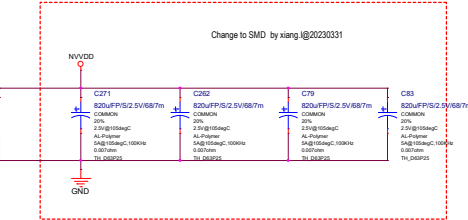
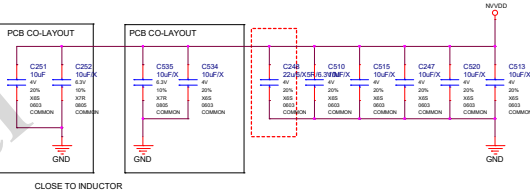
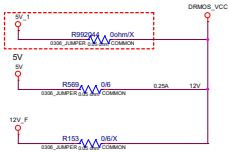




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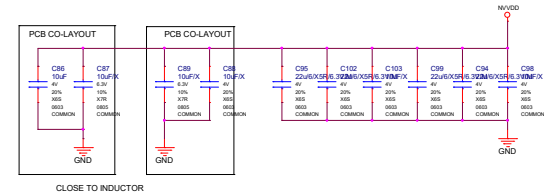
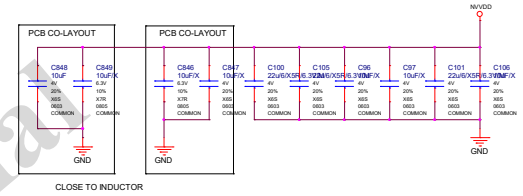


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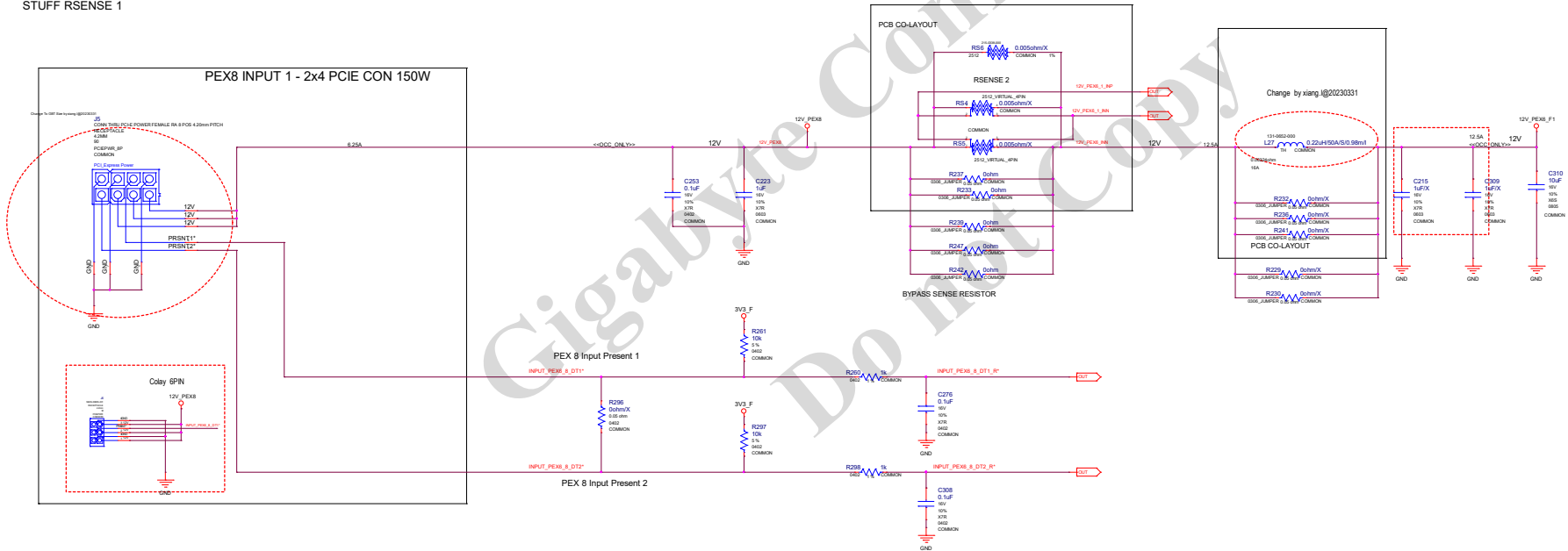
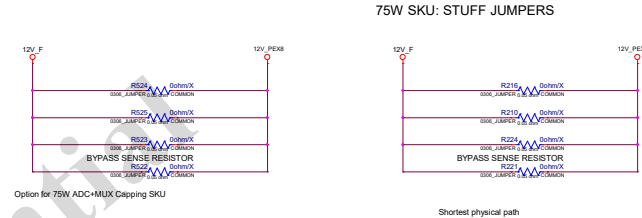
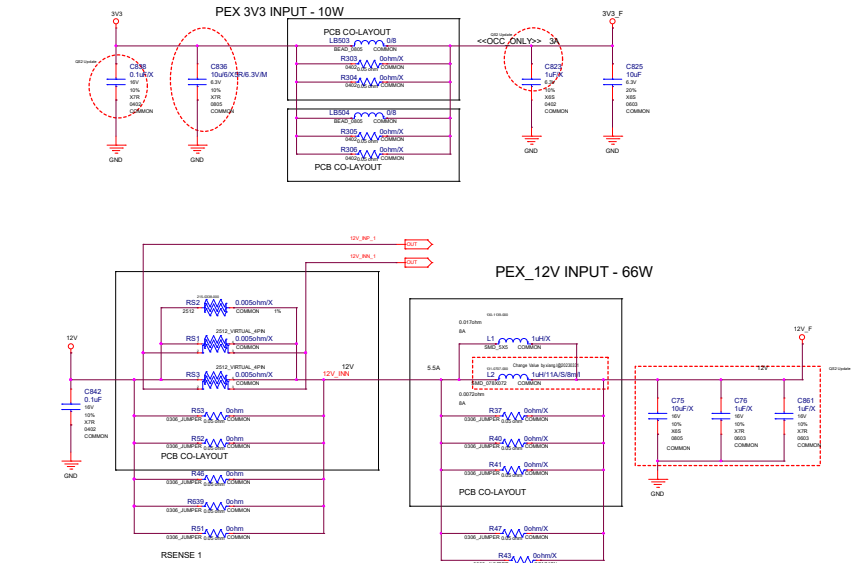
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Power Inputs and Filtering



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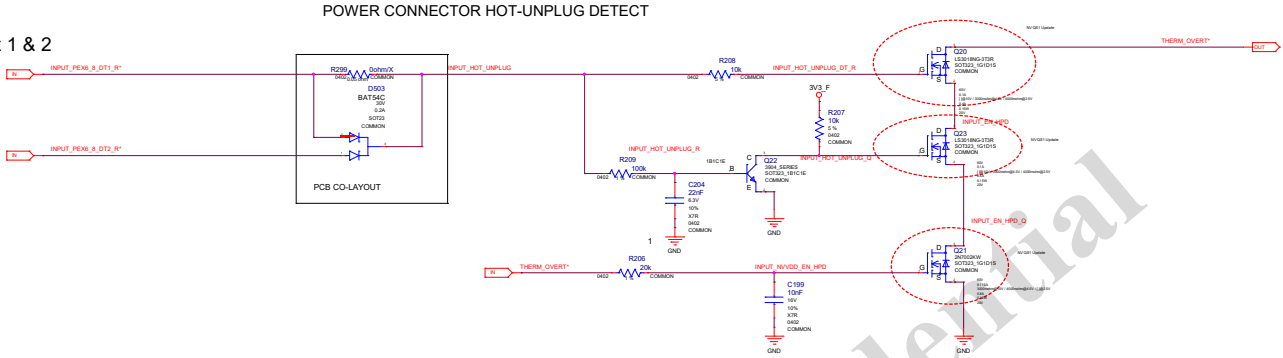
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Power Inputs and Filtering

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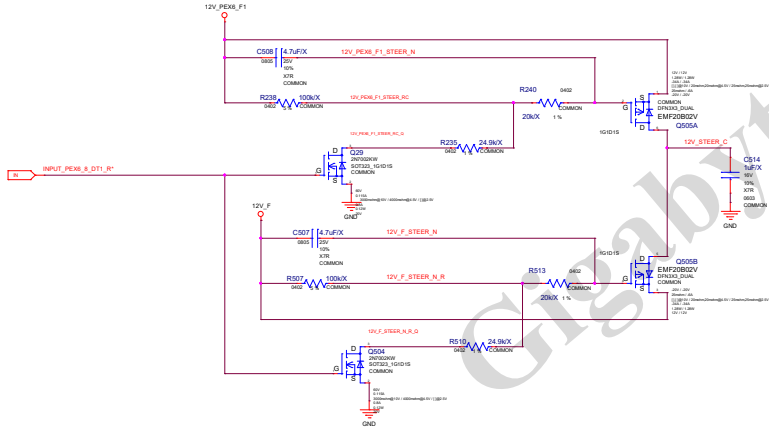
PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG

PEX Input Present 1 & 2

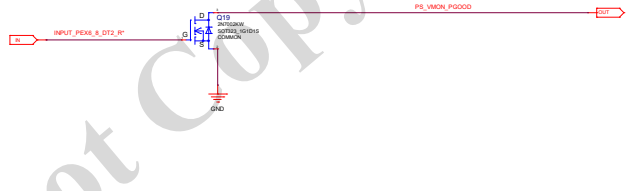


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PCIe 8PIN DETECTION



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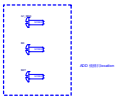
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PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG

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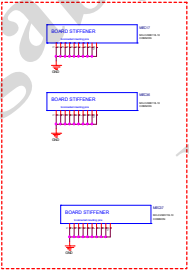
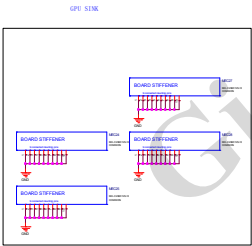


MECH AND EMI CLIPS

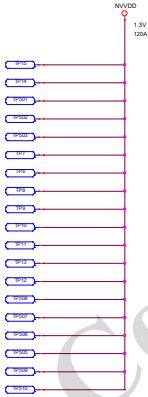
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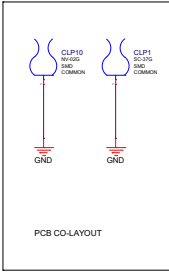
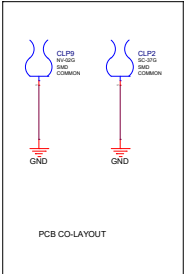
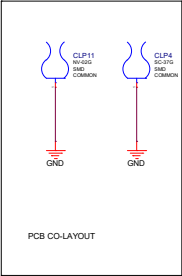
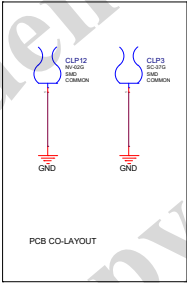
MECH



NVDD OPEN PAD:



EMI CLIP:



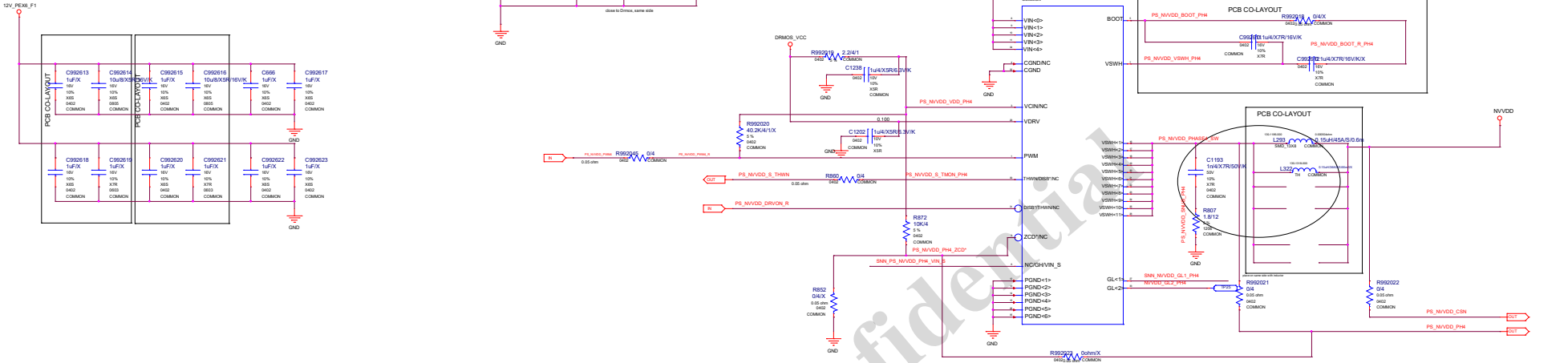
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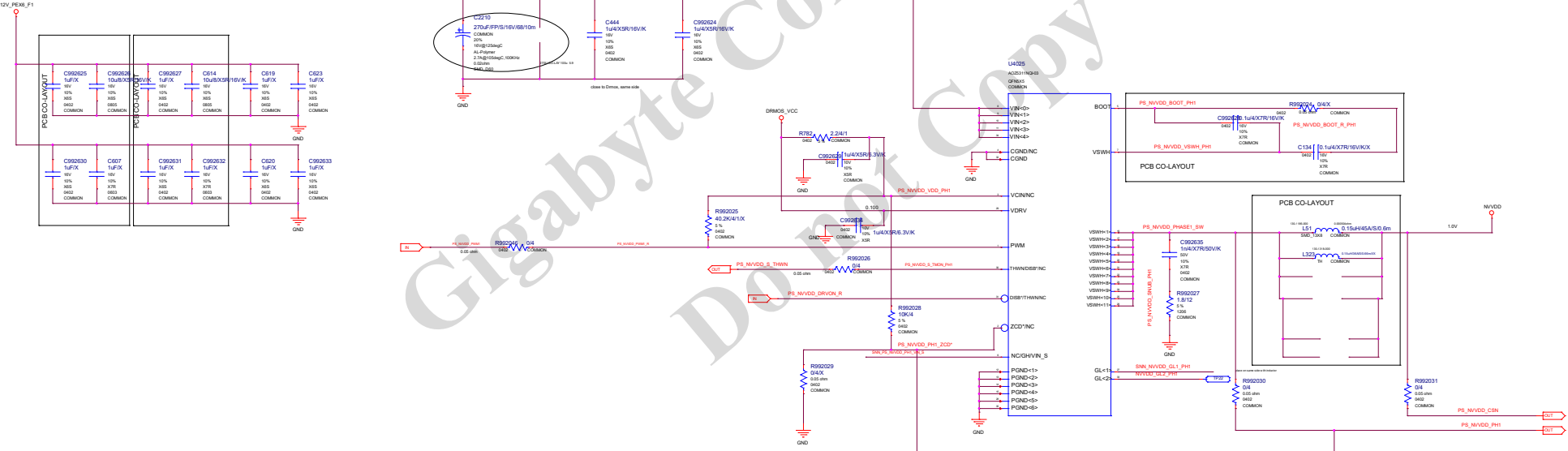
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NVDD PH1 & PH4



NVDD PH1(PWM1)



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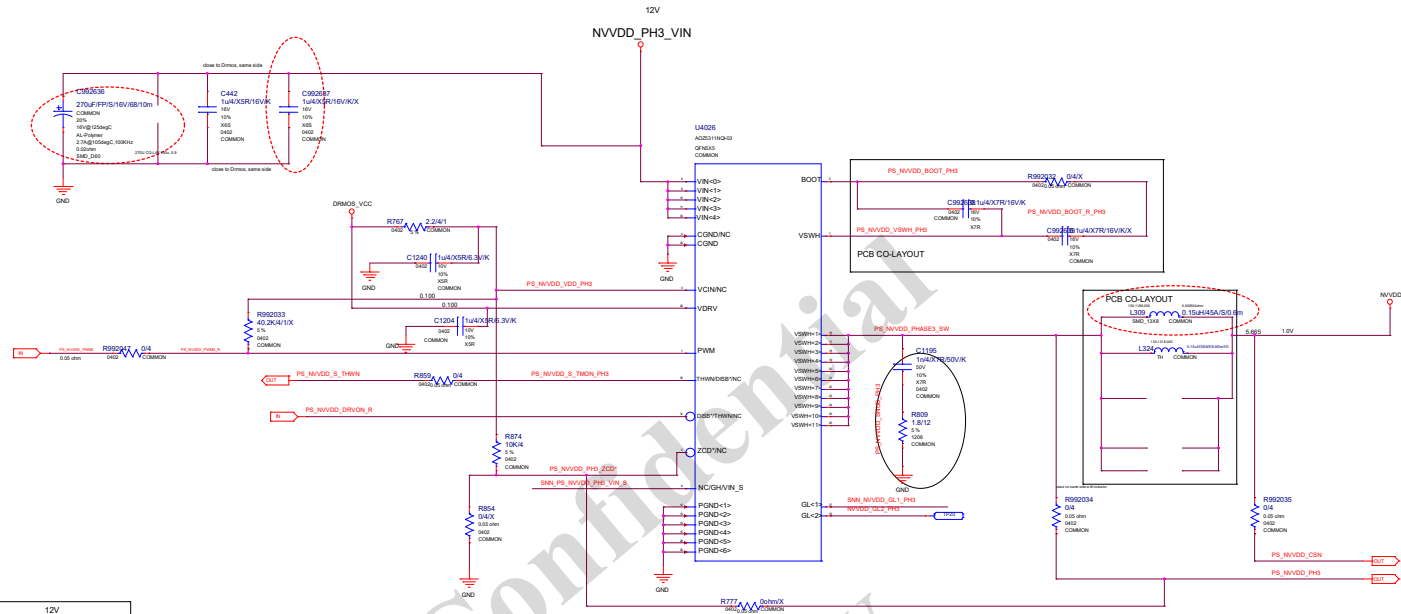
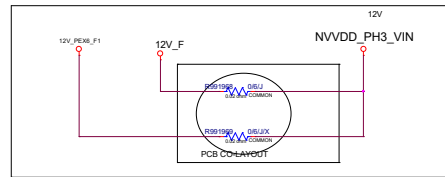
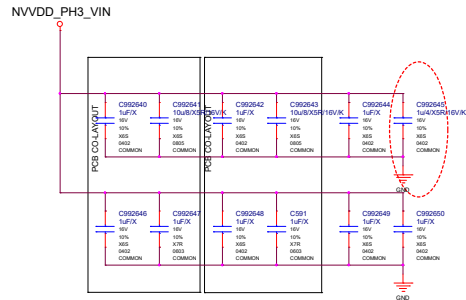
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## MECH AND EMI CLIPS

## NVVDD PH3

NVVDD<sub>12V</sub>PH3(PWM3)

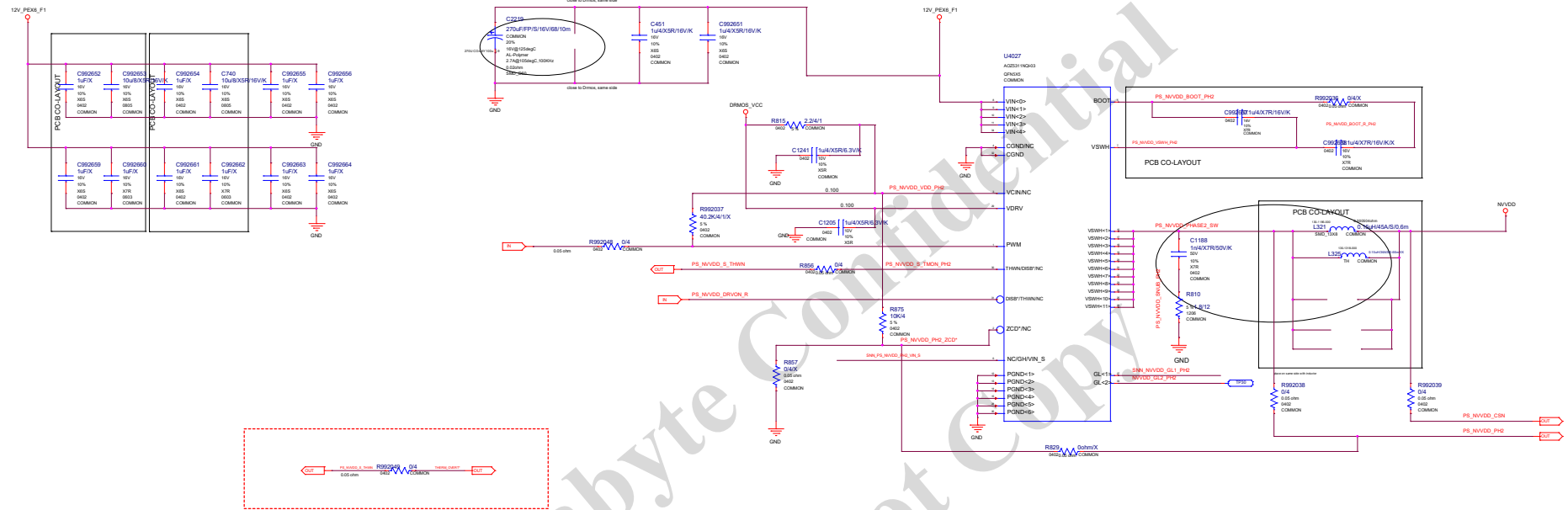
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## MECH AND EMI CLIPS

NVVDD PH2(PWM2)



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**GIGABYTE**

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MECH AND EMI CLIPS

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